REMARKS

Claims 1-21 are pending.

Claims 1-21 are rejected.

Claim 1 has been amended to correct an antecedent basis problem.

I. REJECTION UNDER 35 U.S.C. § 112

Claim 1 is rejected under *35 U.S.C. §* 112, second paragraph, as being indefinite. The Applicant has amended Claim 1 adding "physical layer" before the first and second occurrence of "devices" to correct the antecedent basis problem. Therefore the rejection of Claim 1 under *35 U.S.C. §* 112 second paragraph is traversed by the amendment to Claim 1.

The Applicants respectfully assert that the amendment to Claim 1 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

II. REJECTIONS UNDER 35 U.S.C. § 102

The Office Action rejected Claims 6, 9, 10, 13-14, and 19 under *35 U.S.C. §102(b)* as being anticipated by *Cassing* (C6x solutions for voice over IP gateway, Northcon/98 Conference Proceedings 21-23 Oct. 1998, pages 74-85, (hereafter "*Cassing*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Claim 6 has been amended to add "integrated circuit (IC)" following network processor. The title of the present invention is "Integration of Digital Signal Processor" which clearly implies that the DSP functionality is integrated into another circuit structure. The Summary of the Invention states that the DSP functionality is integrated with a network processor. See page 5, lines 2-3. The Specification, page 3, lines 21-25 describes the problem of having the DSP separate from a network processor chip which defines that the network processor is an IC (chip). Further this recitation describes making a DSP core a part of the network processor architecture and thus a network processor IC.

Network processor 100 is shown in FIG. 1 as having on-chip storage 111 which implies that all of the elements 104, 105, 106, 108-109, and 111 making up network processor 100 are on a single chip or IC. In the Specification, page 9, lines 21-24 it states that the DSPs 401-403 are coupled into the network processor (100) thus are integrated into the network process IC.

These above recitations give support for amending the claims to more clearly recite that Claim 6 is directed to the combination of a network processor and a DSP core in an IC.

The Office Action states that the prior art reference *Cassing* published in October 1998 anticipates Claim 6. The Office Action states that FIG. 4 of *Cassing* is the network processor of Claim 6. *Cassing* describes FIG. 4 as a "DSP Board Architecture" which defines the elements of FIG. 4 as making up a DSP board and not a network processor IC with integrated DSP functionality. FIG. 4 of *Cassing* further shows 5M Bytes of SDRAM, 8M Bytes of DRAM and 4M Bytes of Flash memory. The Applicant asserts that in 1998 this amount of memory would not be integrated on a single IC, thus FIG. 4 cannot be describing a network processor IC with integrated DSP functionality as recited in Claim 6. The Applicant traverses the rejection of Claim 6 over *Cassing* by providing

further evidence that as late as August 2005 the industry states that the network processor and DSPs have not been combined on the same chip (IC). See "Electronicstalk" first paragraph, www.electronicstalk.com/news/age/age183.html which states the following: "These issues centre on various ways digital signal processor (DSP) modem and network processor chips might be integrated in digital subscriber line access multiplexer (DSLAM) equipment. So far these two types of chips –among the industry's most intriguing-have not been combined on the same chip."

Therefore, the Applicant respectfully asserts that the rejection of Claim 6 under *35 U.S.C. §102(b)* as being anticipated by *Cassing* is traversed by the above arguments.

Claims 9 and 10 depend from Claim 6 and contain all the limitations of Claim 6. The Office Action rejected Claims 9 and 10 for the same reasons a Claim 6. The Applicant has shown that *Cassing* does not anticipate Claim 6, therefore, the Applicant respectfully asserts that the rejections of Claims 9-10 under *35 U.S.C. §102(b)* as being anticipated by *Cassing* are traversed for the same reasons as Claim 6.

Amended Claim 13 is an independent method claim directed to 4 method steps for improving the performance and functionality of a network processor IC controlling the communication between physical layer devices. The Office Action rejects Claim 13 as being anticipated by *Cassing*. The Applicant has shown that *Cassing* does not anticipate a network processor IC with an integrated DSP functionality and thus does not anticipate a method for improving the performance of a network processor IC by adding DSP functionality. Therefore, the Applicant respectfully asserts that the rejection of Claims 13 under *35 U.S.C. §102(b)* as being anticipated by *Cassing* is traversed for the same reasons as Claim 6.

Claims 14 and 19 depend from Claim 13 and contain all the limitations of Claim 6. The Office Action rejected Claims 14 and 19 for the same reasons a Claim 13. The Applicant has shown that *Cassing* does not anticipate Claim 13, therefore, the Applicant respectfully asserts that the rejections of Claims 14-19 under *35 U.S.C. §102(b)* as being anticipated by *Cassing* are traversed for the same reasons as Claim 13.

III. REJECTIONS UNDER 35 U.S.C. § 103

To establish a *prima facie* case of obviousness, the Office Action must meet three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.

The Office Action rejected Claims 1-5 under *35 U.S.C. § 103(a)* as being unpatentable over U.S. Patent No. 6,987,756 to *Ravindranath et al.* (hereafter "*Ravindranath*") in view of *Wolf et al.* (Design Issues for High-Performance Active Routers. Selected Areas in Communications, IEEE Journal, Volume 19, Issue 3, March 2001 pages 404-409) (hereafter "*Wolf*").

Claim 1 has been amended to make it clear that the digital signal processor (DSP) is in the integrated circuit (IC) for data communication. The IC of Claim 1 comprises a digital signal processor, circuitry for receiving digital signals from physical layer devices within a communication network, circuitry for receiving analog signals from a selected one of said physical layer devices, circuitry for routing said analog and digital signals to said DSP, said DSP outputting processed signals in response to DSP programming commands, circuitry for incorporating particular processed digital signals into data packets corresponding to a communication protocol, and circuitry for receiving and transmitting said data packets of a communication protocol to and from a network coupling said physical layer devices.

The circuitry of Claim 1 describes the functionality of a network processor integrated with a DSP in a single integrated circuit. The Applicant has shown that a single IC containing a network processor and the functionality of a DSP was not known in 1999 when the Application of *Ravindranath* was filed and when *Wolf* was published in March of 2001. The Applicant has shown evidence that as late as August 2005 the industry states that the network processor and DSPs have not been combined on the same

integrated circuit chip (IC) citing "Electronicstalk" first paragraph, www.electronicstalk.com/news/age/age183.html. Further, *Ravindranath* does not mention a network processor in his disclosure. There is no teaching or suggestion in *Ravindranath* to combine the functionality of a network processor with a DSP on a single IC. Therefore the Applicant asserts that *Ravindranath* and *Wolf*, singly or in combination do not teach or suggest the invention of Claim 1.

Therefore, the Applicant asserts that the rejection of Claim 1 under *35 U.S.C. § 103(a)* as being unpatentable over *Ravindranath* in view of *Wolf* is traversed for the above arguments and for the same reasons as Claim 6.

Claims 2-5 are directly or indirectly dependent from Claim 1 and contain all the limitations of Claim 1; specifically that the functionalities of Claims 2-5 are incorporated into an IC that is the combination of a DSP and the functionality of a network processor. The Applicant has shown that *Ravindranath* and *Wolf*, singly or in combination, do not teach or suggest the invention of Claim 1. The Applicant, therefore, asserts that *Ravindranath* and *Wolf*, singly or in combination, do not teach or suggest the inventions of Claims 2-5.

Therefore, the Applicant asserts that the rejections of Claims 2-5 under *35 U.S.C. § 103(a)* as being unpatentable over *Ravindranath* in view of *Wolf* is traversed for the above arguments and for the same reasons as Claim 1 and 6.

The Office Action rejected Claims 7-8 and 16-18 under *35 U.S.C. § 103(a)* as being unpatentable over *Cassing* in view of U.S. Patent No. 6,987,756 to *Chan et al.* (hereafter "*Chan*").

The Applicant has shown that when *Cassing* was published and when *Chan* was filed, June 2001, no one had integrated a network processor and DSP functionality on a single integrated circuit (IC). *Chan* describes a network appliance and does not teach or suggest combining a network processor with a DSP on a single IC. Therefore, the

Applicant asserts that one of ordinary skill in the art could not combine the teachings of *Cassing* and *Chan* to arrive at the invention of Claim 6.

Claim 7 is dependent from Claim 6 and contains all the limitations of Claim 6. Claim 7 adds the limitation that one of the processors in the EPC in the single IC is the DSP. The Office Action states that *Cassing* does not explicitly teach that the DSP is one of the processors in the EPC. The Office Action states that *Chan* teaches a network processor and DSP functions in a network appliance. The Applicant has shown that the prior art did not teach or suggest combining a network processor and DSP on a single IC at the time the invention of *Chan* was filed. The Applicant asserts that *Cassing* and *Chan*, singly or in combination, do not teach the invention of Claim 7. The Office Action rejects Claims 8 and 16-17 for the same reasons as Claim 7. Therefore, the Applicants further assert that the rejections of Claims 7-8 and 16-17 under *35 U.S.C. § 103(a)* as being unpatentable over *Cassing* in view of *Chan* are traversed by the above arguments and the same reasons as Claim 6.

The Office Action rejected Claims 11-12, 15, and 20-21 under *35 U.S.C. § 103(a)* as being unpatentable over *Cassing* in view of *Ravindranath*.

The Office Action rejects Claims 11 and 12 for the same reasons. Claim 11 is dependent from Claim 6 and contains all the limitations of Claim 6. The Applicant has shown that *Cassing* and *Ravindranath*, singly or in combination, do not teach the invention of Claim 6. The Office Action states that *Cassing* does not explicitly teach that the limitations of Claims 11 and 12. However, the Office Action states that *Ravindranath's* teaching that processor 345 controls the compression algorithm used by the DSP is the same as a DSP combined with a network processor on a single IC receiving program commands via the switch fabric from a remote device through a general purpose processor as recited in Claim 11. The Applicant asserts that *Ravindranath* does not teach or suggest the limitation of Claim 11. Further, *Ravindranath* does not teach or suggest that the DSP receives program commands from a

general purpose processor that is on the same chip as the network processor as recited in Claim 12.

Therefore, the Applicant asserts that the rejections of Claims 11-12 under *35 U.S.C. § 103(a)* as being unpatentable over *Cassing* in view of *Ravindranath* are traversed for the above arguments and for the same reasons as Claim 6.

Claims 15 and 20-21 are dependent from Claim 13 and contain all the limitations of Claim 13. The Applicant has shown that *Cassing* and *Ravindranath*, singly or in combination, do not teach the invention of Claim 13. The Office Action does not specifically address Claims 15 and 20-21 relative to the rejections *U.S.C. § 103(a)* as being unpatentable over *Cassing* in view of *Ravindranath* and therefore fails to make a prima facie case of obviousness.

Therefore, the Applicant asserts that the rejections of Claims 15 and 20-21 under *35 U.S.C. § 103(a)* as being unpatentable over *Cassing* in view of *Ravindranath* are traversed by the above argument.

IV. CONCLUSION

Claims 1, 6-14, 16-18, and 20-21 have been amended.

The rejection of Claim 1 under *35 U.S.C. §* 112 second paragraph has been traversed.

The rejection of Claims 6, 9, 10, 13-14, and 19 under *35 U.S.C. §102(b)* as being anticipated by *Cassing* have been traversed.

The rejections of Claims 1-5 under *35 U.S.C. § 103(a)* as being unpatentable over *Ravindranath* in view of *Wolf* have been traversed.

The rejections of Claims 7-8 and 16-18 under *35 U.S.C. § 103(a)* as being unpatentable over *Cassing* in view of *Chan* have been traversed.

The rejections of Claims 11-12, 15, and 20-21 under *35 U.S.C. § 103(a)* as being unpatentable over *Cassing* in view *Ravindranath* have been traversed.

The Applicant, therefore, respectfully asserts that Claims 1-21 are now in condition for allowance and requests an early allowance of these claims.

Applicants respectfully request that the Office Action call Applicant's attorney at the below listed number if the Office Action believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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